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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,587	01/28/2004	Miwa Wake	S004-4839	3839

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EXAMINER

TRAN, THANH Y

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/766,587

Applicant(s)

WAKE ET AL.

Examiner

Thanh Y. Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 July 2006.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-6 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 2 and 3 is/are allowed.
6) ☒ Claim(s) 4-6 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohsawa (U.S. 2002/0051378).

As to claim 4, Ohsawa discloses in figure 49 a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film (having n-type and p-type regions as shown in figure 49) provided on a first conductivity type supporting substrate (10) through an embedded insulating film ("silicon oxide film" 11), comprising: a second conductivity type source region (having p-type in source region as shown in figure 49) and a second conductivity type drain region (having p-type in drain region as shown in figure 49) formed in the semiconductor film; a gate insulating film (16) formed on an upper surface of the semiconductor film; and a gate electrode (13) formed on an upper surface of the gate insulating film (16), wherein the source region (14a, 14b) includes an ultra-shallow high-density N-type source extension region (14b) at a boundary with a channel region, a low-density N-type source extension region (14a) under the ultra-shallow high-density N-type source region (14b), and an embedded insulating (11) neighboring N-type source extension region, the source extension regions (14a, 14b) being stacked in a thickness direction of the semiconductor film; and wherein

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the drain region includes an ultra-shallow high-density N-type drain extension region (14b) at a boundary with the channel region, a low-density N-type drain extension region (14a) under the ultra-shallow high-density N-type drain extension region (14b), and an embedded insulating (11) neighboring N-type drain extension region (15a, 15b), the drain extension regions (15a, 15b) being stacked in a thickness direction of the semiconductor film.

As to claim 5, Ohsawa discloses in figure 49 a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film (having n-type and p-type regions as shown in figure 49) provided on a first conductivity type supporting substrate (10) through an embedded insulating film ("silicon oxide film" 11), further comprising: a first sidewall (element 17 on the left side of electrode 13) disposed around the gate electrode (13) and a second sidewall (element 17 on the right side of electrode 13) disposed on the first sidewall.

As to claim 6, Ohsawa discloses in figure 40 a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film (having p-type regions as shown in figure 40) provided on a first conductivity type supporting substrate (10) through an embedded insulating film ("silicon oxide film" 11), comprising: a second conductivity type source region (15) and a second conductivity type drain region (14) formed in the semiconductor film (11); a gate insulating film ("gate oxide film" 16) formed on an upper surface of the semiconductor film (11); and a gate electrode (13) formed on an upper surface of the gate insulating film (16), wherein a channel region (comprising regions 12a, 12b) disposed under the gate insulating film (16) has a first conductivity type impurity region (12b) having a higher density ("concentration") than a well (12a) at a boundary with the drain region (region of

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15) [region 12b has a high density (concentration), but region 12a has a low concentration (low density)] (see paragraph [0289]).

Allowable Subject Matter

3. Claims 2-3 are allowed.

4. The following is an examiner's statement of reasons for allowance:

The prior art of record and to the examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding:

A method of manufacturing a semiconductor integrated circuit, in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film, comprising the steps of: conducting thermal oxidation to form a LOCOS for element separation between transistors in the semiconductor film; forming a second conductivity type impurity region in an ultra-shallow portion of each of a source region and a drain region; forming a second conductivity type impurity region having a low density in a middle portion of each of the source region and the drain region; forming a second conductivity type impurity region having the same density as the second conductivity type impurity region in the ultra-shallow portion in a lower portion of each of the source region and the drain region, as recited in claim 2

A method of manufacturing a semiconductor integrated circuit, in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film, comprising the steps of: conducting thermal oxidation to form a LOCOS for element separation between transistors in the semiconductor film; forming a first conductivity type impurity region having a

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higher density than that of the first conductivity type impurity region in a middle depth portion of the semiconductor film serving as the proximal region to a drain in the first conductivity type impurity region; and performing ion implantation through the gate electrode so as to form a second conductivity type impurity region in each of a source region and a drain region, as recited in claim 3.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant's arguments with respect to claims 4-6 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that drain regions 14a, 14b of Ohsawa are stacked or extend along a length, not a thickness, direction of an insulating film 11.

In response, the examiner disagrees with applicant's argument because figure 49 of Ohsawa clearly discloses the source regions (14a, 14b) and the drain regions (15a, 15b) are extended in a thickness of the semiconductor film (a semiconductor film is a layer that is formed between layers 18 and 11, the source and drain regions are included in the semiconductor film). Since semiconductor film is a 3-dimension element/film, it inherently has a thickness.

Conclusion

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6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Contact Information

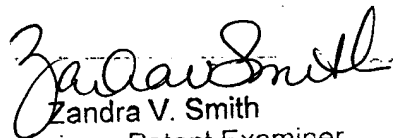
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT 10/766,587


Zandra V. Smith
Supervisory Patent Examiner
2 Oct 2009